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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,514	07/11/2003	Imran Khan	AMD-H0552	6596

7590 12/28/2004

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EXAMINER

KEBEDE, BROOK

ART UNIT PAPER NUMBER

2823

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/618,514

Applicant(s)

KHAN ET AL.

Examiner

Brook Kebede

Art Unit

2823

*AK*

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 18 October 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) 20 and 21 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 11-19 is/are allowed.
- 6) ☒ Claim(s) 1,2,9 and 10 is/are rejected.
- 7) ☒ Claim(s) 3-8 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 9 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Fang et al. (US/6,818,519).

Re claim 1, Fang et al. disclose a method of fabricating a semiconductor device having a triple LDD (lateral diffused dopants) structure, comprising: forming a gate structure (36A 36B, i.e., 36) on a surface of a semiconductor substrate (12), wherein said gate structure (36) includes a first vertical surface and a second vertical surface (i.e., the gate pattern 38A 38B, i.e., 38, having two vertical side walls as depicted in Fig. 6A); forming a first spacer (40A 40B 40C 40D) adjacent to said first vertical surface (i.e., the first spacer 40A 40B 40C 40D, i.e., 40, formed on the first vertical sidewall of gate pattern 38), a second spacer (42A 42B 42C 42D, i.e., 42) adjacent to said second vertical surface (i.e., the second spacer 42 formed on the second sidewall of the gate 36), wherein said first spacer (40) has a first thickness and a second thickness that is greater than said first thickness and that abuts said first vertical surface (i.e., the first spacer 40 on the first sidewall of the gate 36 has higher thickness in the bottom side of the gate 36 than that of the tope side of the gate 36) (see Fig. 6A), and wherein said second spacer (42) has a third thickness and a fourth thickness that is greater than said third thickness and that abuts said

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second vertical surface (i.e., ; and the second spacer 42 on the second sidewall of the gate 36 has higher thickness in the bottom side of the gate 36 than that of the top side of the gate 36) (see Fig. 6A) performing a single implant process to form said triple LDD structure(46 44 48) for a drain and a source of said semiconductor device in said semiconductor substrate (see Figs. 5 and 6A).

Re claim 2, as applied to claim 1 above, Fang et al. teach all the claimed limitation including the limitation performing a silicidation process such that a silicide is formed on a horizontal surface of said gate structure, a first upper portion of said first vertical surface, and a second upper portion of said second vertical surface, i.e., the conventional silicidation process followed after the step 40 as depicted in Fig. 5 (see Figs. 5 and 6A).

Re claim 9, as applied to claim 1 above, Fang et al. teach all the claimed limitation including the limitation wherein said implant process is an ion implant process (see Figs. 5 and 6A).

Re claim 10, as applied to claim 1 above, Fang et al. teach all the claimed limitation including the limitation wherein said semiconductor device is a MOSFET (metal oxide semiconductor field effect transistor) (see Figs. 5 and 6A).

***Allowable Subject Matter***

3. Claims 3-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
4. Claims 11-19 are allowed over prior art of record.

***Response to Arguments***

5. Applicants' arguments with respect to claims 1, 2, 9, and 10 have been considered but are moot in view of the new ground(s) of rejection that was necessitated by the amendment filed on October 18, 2004.

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure Zhou et al. (US/6,156,598) and Kim (US 2002/0158289) also disclose slimier inventive subject matter.

7. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


*Correspondence*

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK  
December 17, 2004

  
George Fourson  
Primary Examiner